1. A method of characterizing a device under test, the method comprising:

injecting a signal into the device under test;

measuring the response to the injected signal to determine the impedance of the device under test in the frequency domain;

converting the impedance of the device under test to a time domain; and

calculating the voltage noise of the device under test based on the impedance in the time domain.

2. The method of claim 1 in which the step of measuring the response includes constructing an s-parameter matrix and calculating the real and imaginary portions of the impedance of the device under test as a function of frequency based on the s-parameter matrix.

3. The method of claim 2 in which the step of construction the s-parameter matrix includes establishing calibration data, generating an uncorrected s-parameter matrix based on the measured impedance of the device under test, and applying the calibration data to the uncorrected s-parameter matrix to produce a corrected s-parameter matrix.

4. The method of claim 1 in which converting includes performing an

inverse Fourier transform on the impedance in the frequency domain.

5. The method of claim 1 in which calculating the voltage noise of the device under test includes convolving the impedance in the time domain with a predetermined current in the time domain.

6. The method of claim 1 in which the impedance determined is self-impedance.

7. The method of claim 6 in which the step of determining the impedance of the device under test includes measuring, at a terminal pair of the device under test using one test port of an analyzer, the response to a signal input to the terminal pair from a different test port of the analyzer.

8. The method of claim 1 in which the impedance determined is the transfer impedance.

9. The method of claim 8 in which the step of determining the impedance of the device under test includes measuring, at one terminal pair of the device under test using one test port of an analyzer, the response to a signal input to a different terminal pair of the device under test from a different test port of the analyzer.

10. The method of claim 1 in which the voltage noise calculated is the

simultaneous switching noise.

11. The method of claim 10 in which the step of determining the impedance of the device under test includes injecting an input signal to a plurality of terminal pairs of the device under test.

12. The method of claim 11 in which the voltage noise at a particular terminal pair of interest on the device under test is calculated and the simultaneous switching noise is the sum of all voltage noise signals.

13. The method of claim 1 in which the device under test has multiple terminal pairs and the timing of calculated voltage noise of each terminal pair is adjusted until a maximum total voltage noise is achieved to determine a worst case scenario concerning timing of the signal input to each terminal pair and the resulting total voltage noise.

14. The method of claim 1 further including the step of determining the spectral response of the device under test.

15. The method of claim 14 in which the step of determining the spectral response of the device under test includes performing a Fourier transform on the calculated voltage noise of the device under test.

16. The method of claim 1 in which the device under test is a printed circuit board.

17. The method of claim 1 in which the device under test is an integrated circuit package.

18. The method of claim 1 in which the device under test is an interconnect component.

19. The method of claim 1 in which the device under test is a digital representation of a physical device and the injected signal and measured response are simulated.

20. A method of characterizing a device under test, the method comprising:

determining the impedance of the device under test in the frequency domain by constructing an s-parameter matrix and calculating the real and imaginary portions of the impedance based on the s-parameter matrix;

converting the frequency domain impedance of the device under test to a time domain by performing an inverse Fourier transform on the determined complex impedance; and

calculating the voltage noise of the device under test by convolving the time domain impedance with a predetermined current in the time domain.

21. The method of claim 20 in which determining the impedance includes injecting a signal into the device from one or more test ports of an analyzer and measuring the response of the device.

22. The method of claim 20 in which the predetermined current is a current specified for the device under test.

23. The method of claim 20 in which the step of constructing the s-parameter matrix includes establishing calibration data, generating an uncorrected s-parameter matrix based on the measured impedance of the device under test, and applying the calibration data to the uncorrected s-parameter matrix to produce a corrected s-parameter matrix.

24. The method of claim 20 in which the impedance determined is self-impedance.

25. The method of claim 20 in which the step of determining the impedance of the device under test includes measuring, at a terminal pair of the device under test using one test port of an analyzer, the response to a signal input to the terminal pair from a different test port of the analyzer.

26. The method of claim 20 in which the impedance determined is the transfer impedance.

27. The method of claim 26 in which the step of determining the impedance of the device under test includes measuring, at one terminal pair of the device under test using one test port of an analyzer, the response to a signal input to a different terminal pair of the device under test from a different test port of the analyzer.

28. The method of claim 20 in which the voltage noise calculated is the simultaneous switching noise.

29. The method of claim 28 in which the step of determining the impedance of the device under test includes measuring the response of a plurality of terminal pairs of the device under test.

30. The method of claim 29 in which the voltage noise of each terminal pair of the device under test is calculated and the simultaneous switching noise is the sum of the voltage noise of each terminal of the device under test.

31. The method of claim 20 in which the device under test has multiple terminal pairs, a signal is input to each terminal pair, and the calculated voltage noise of each terminal pair is adjusted until a maximum total voltage noise is achieved to determine a worst case scenario concerning timing of the signal input to each terminal pair and a resulting total voltage noise.

32. The method of claim 20 further including the step of determining the spectral response of the device under test.

33. The method of claim 32 in which the step of determining the spectral response of the device under test includes performing a Fourier transform on the calculated voltage noise of the device under test.

34. The method of claim 20 in which the device under test is a printed circuit board.

35. The method of claim 20 in which the device under test is an integrated circuit package.

36. The method of claim 20 in which the device under test is an interconnect component.

37. The method of claim 20 in which the device under test is a digital representation of a physical device.

38. A system for characterizing a device under test, the system comprising:

an input subsystem configured to inject a signal into the device under test and measure the response of the device under test;

a routine responsive to the input subsystem for characterizing the frequency domain impedance of the device under test;

a routine configured to convert the frequency domain impedance to a time domain impedance; and

a routine configured to calculate the voltage noise of the device under test based on the time domain impedance.

39. The system of claim 38 in which the input subsystem includes a network analyzer.

40. The system of claim 39 in which the network analyzer includes a plurality of test ports connectable to the device under test for injecting a signal into the device under test and receiving a response from the device under test.

41. The system of claim 38 further including an output device for outputting the calculated voltage noise of the device.

42. The system of claim 38 further including a user interface for inputting a current specified for the device under test.

43. The system of claim 38 in which the routine for characterizing the frequency domain impedance is configured to construct an s-parameter matrix and to calculate the real and imaginary portions of the impedance based on the s-parameter matrix.

44. The system of claim 43 further including a calibration routine for establishing calibration data, an uncorrected s-parameter matrix is based on the measured impedances of the device under test, and the calibration data is applied to the uncorrected s-parameter matrix to produce a corrected s-parameter matrix.

45. The system of claim 38 in which the routine configured to convert the frequency domain impedance to a time domain impedance performs an inverse Fourier transform on the frequency domain impedance.

46. The system of claim 38 in which the routine for calculating the voltage noise of the device under test convolves the time domain impedance with a predetermined current.

47. The system of claim 38 in which the impedance determined is self-impedance.

48. The system of claim 38 in which the input subsystem is configured to measure, at a terminal pair of the device under test using one test port of the input

subsystem, the response to a signal input to the terminal pair from a different test port of the input subsystem.

49. The system of claim 38 in which the impedance determined is the transfer impedance.

50. The system of claim 49 in which the input subsystem is configured to measure, at one terminal pair of the device under test using one test port of the input subsystem, the response to a signal input to a different terminal pair of the device under test from a different test port of the input subsystem.

51. The system of claim 38 in which the voltage noise calculated is the simultaneous switching noise.

52. The system of claim 51 in which the input subsystem is configured to input a signal to a plurality of terminal pairs of the device under test.

53. The system of claim 52 in which the voltage noise at a particular terminal pair of interest on the device under test is calculated and the simultaneous switching noise is calculated as the sum of all voltage noise signals.

54. The system of claim 38 in which the device under test has multiple terminal pairs, a signal is input to each terminal pair by the input subsystem, and the

voltage noise at a particular terminal pair of interest is calculated and the timing of the input signals is adjusted until a maximum total voltage noise is achieved to determine a worst case scenario concerning timing of the signal inputs to each terminal pair and a resulting total voltage noise.

55. The system of claim 38 further including a routine for determining the spectral response of the device under test.

56. The system of claim 55 in which the routine for determining the spectral response of the device under test performs a Fourier transform on the calculated voltage noise of the device under test.

57. The system of claim 38 in which the device under test is a printed circuit board.

58. The system of claim 38 in which the device under test is an integrated circuit package.

59. The system of claim 38 in which the device under test is an interconnect component.

60. The system of claim 38 in which the device under test is a digital representation of a physical device and the input subsystem simulates an injected signal

and a response.

61. A system for characterizing a device under test, the system comprising:

a routine for determining the frequency domain impedance of the device under test by constructing an s-parameter matrix and calculating the real and imaginary portions of the impedance based on the s-parameter matrix;

a routine for converting the frequency domain impedance to a time domain impedance by performing an inverse Fourier transform on the complex impedance; and

a routine for calculating the voltage noise of the device under test by convolving the time domain impedance with a predetermined current.

62. The system of claim 61 in which further including an analyzer configured to inject a signal into the device from one or more test ports and to measure the response of the device.

63. The system of claim 61 in which the predetermined current is a current specified for the device under test.

64. A system for characterizing a device under test, the system comprising:

an input subsystem configured to inject a signal into the device under test and to measure the response of the device under test; and

a routine for automatically determining the frequency domain impedance of the device under test by constructing an s-parameter matrix and calculating the real and imaginary portions of the impedance based on the s-parameter matrix.

65. The system of claim 64 further including a routine for converting the frequency domain impedance to a time domain impedance by performing an inverse Fourier transform on the complex impedance.

66. The system of claim 65 further including a routine for calculating the voltage noise of the device under test by convolving the time domain impedance with a predetermined current.